IN THE SPECIFICATION

*Please replace paragraph **[0024]** with the following amended paragraph:*

[0024] In a next step, a flowable dielectric layer 220 is formed over the resultant structure by using a spin on dielectric (SOD) such as a silicate, a siloxane, a methyl SilsesQuioxane (MSQ), a hydrogen SisesQuioxane(HSQ), an MSQ/HSQ, a perhydrosilazane (TCPS) or a polysilazane. Alternatively, the flowable dielectric layer 220 can be formed by using a low temperature undoped dielectric at a temperature in a range of about -10 °C [[_]] to about 150 °C [[_]] under a pressure ranging from about 10 mTorr to about 100 Torr, wherein a reaction source uses a mixture gas of $SiH_x(CH_3)_y$ ($0 \leq x \leq 4$, $0 \leq y \leq 4$), H_2O_2, O_2, H_2O and N_2O. It is preferable that the thickness of the flowable dielectric layer 220 is in the range of about 1,000 °C [[_]] to about 20,000 °C [[_]] in consideration of heights of the gates 216 and a gap space between the gates 216.

*Please replace paragraph **[0025]** with the following amended paragraph:*

[0025] After forming the flowable dielectric layer 220, referring to Fig. 3B, an annealing process is carried out in a furnace at a temperature ranging from about 300 °C [[_]] to about 1,000 °C [[_]] , for densifying the flowable dielectric layer 220 and for removing moisture therein. During the annealing process, there a plurality of micro-pores 215 are formed in the flowable dielectric layer 220. In detail, during the annealing process, a chemical reaction occurs in the flowable dielectric layer 220. That is, silane (SiH_4) and hydrogen peroxide (H_2O_2) interact in the flowable dielectric layer 220, to thereby produce Si-O bonds and O-H bonds. Therefore, O-H bonds again interact with each other to form a byproduct of water (H_2O) by means of a dehydration reaction. The water produced during the dehydration reaction is removed during the annealing process so that a plurality of micro-pores 215 are formed in the flowable dielectric layer 220. In particular, a top face of the flowable dielectric layer 220 is shrunk to condense the flowable dielectric layer 120 so that the micro-pores 215 are rarely formed in a top region thereof. However, since a bottom face of the flowable dielectric layer 220 is fixed to a wafer surface, a bottom region of the flowable dielectric layer 220 is hardly shrunk, whereby the micro-pores 215 are formed during the annealing process.

*Please replace paragraph **[0029]** with the following amended paragraph:*

[0029] Thereafter, referring to Fig. 3D, a barrier layer 226 is formed on bottom faces and sidewalls of the patterned flowable dielectrics 220A and the bottom faces of the contact holes 201 with a thickness in the range of about 20 °C [[_]] to about 300 °C [[_]] preventing a gas or a solution infiltrating into the micro-pores in the patterned flowable dielectrics 220A. Herein, the barrier layer 226 uses a material such as a silicon nitride, a silicon oxide, a silicon carbide or the like.